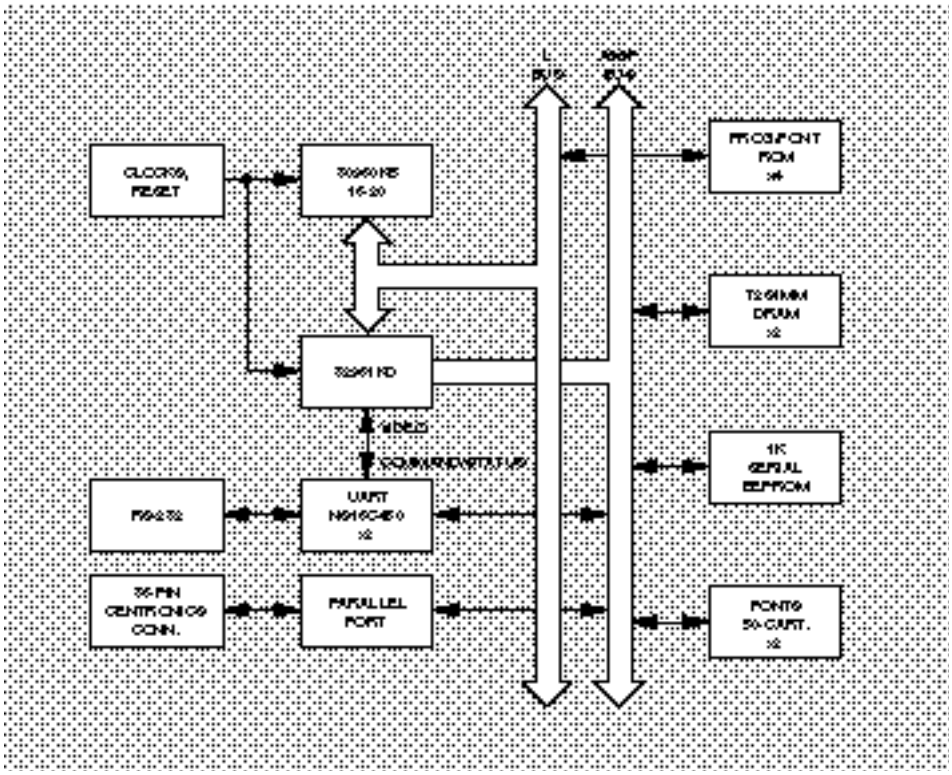
iLASER961KD Laser Printer Controller Design Package

- 20 MHz System Speed
- 4 MB of Interleaved ROM
- Program Memory; Burst Access 3, 0, 2, 0 Wait-State
- Optional 4 MB of Non-Interleaved Flash Memory for Additional Emulations and Fonts
- 4 MB of DRAM Expandable to a Maximum of 32 MB
- 2, 1, 1, 1 Wait-State DRAM
- Supports High Performance 600 dpi Print Engines
- Support Two Font Cartridges
- Two Serial Ports and One Centronics Port



The iLaser961KD page-printer controller is an enabler to high resolution 600 x 600 dpi printing at a low cost. The board is designed to be a printer-resident controller that illustrates how simple an i960/82961KD processor-based design may be. The controller will directly interface to the 17 ppm, Canon NX print engines. The iLaser961KD is designed for both PCL* and PDL applications. The main goal of this controller is to provide a design example to demonstrate how the i960® processor and 82961KD printer coprocessor achieve the high speed printing with less memory required by traditional printers.

The 82961KD on this controller board provides banding capability and bit mapped image compression to more efficiently utilize the page image memory. A hardware BIT-BLT accelerator is also implemented on the 82961KD to greatly increase the print performance. Image compression is achieved using “Scanline Tables.” The memory required for storage of bit mapped images such as character font cache and graphics objects – is significantly reduced by using these structures. The chip’s compressed display list, coupled with its fast graphics operations, allow band buffered printing of very complex page description language (PDL) pages such as those PostScript generates.

With the register programmability on the 82961KD, iLaser961KD controller can be easily turned into a line of printers such as high resolution and color printers based on one single hardware design with no additional software investment. Both ROM and DRAM configurations such as bank size, type, timing, and base addresses, are programmable through internal registers on the 82961KD. The iLaser961KD has two banks of program memory which include one bank of ROM and one bank of Flash. The wait-state profile for ROM is 3,0,2,0 at 20 MHz with interleaved operation. Each board has eight banks of 70 ns DRAM configured as 1M x 32 to achieve 2,1,1,1 wait-states for burst accesses. Eight 72-pin SIMM sockets are on-board for a maximum total of 32 Mbytes DRAM. The controller board also contains two font cartridges, two R-S232 serial interface and a Centronics-compatible parallel interface.

PROCESSORS SUPPORTED:
i960 Processor Family

CONTACT:
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